CLAIMS

What is claimed is:

1. An apparatus generating an error flag, the apparatus comprising:

a frame-sync error memory which stores frame-sync error information for at least one data block;

a BIS (Burst Indicator Subcode) error flag memory which stores a BIS error flag for the at least one data block; and

an error flag generator, which generates an error flag indicating an error existence/absence for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

2. The apparatus of claim 1, wherein the frame-sync error memory stores frame-sync error information corresponding to at least two data blocks.

3. The apparatus of claim 1, wherein the at least one data block has an error correction format in which frame-sync data is recorded in a heading of the at least one data block and BIS data columns are recorded between sets of ECC data columns, and

the error flag generator generates an error flag indicating an error existence for an entire ECC data constructing a set of ECC data columns with reference to error information stored in the frame-sync error memory and the BIS error flag memory, if both the frame-sync error information of the frame-sync data and the BIS error flag of one of the BIS data columns neighboring a set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring a pair of ECC data columns, indicate the error existence.

4. The apparatus of claim 1, further comprising a frame-sync detector, which receives a reproduced digital signal for the at least one data block, determines the error existence/absence for frame-sync data for the at least one data block, and outputs frame-sync error information to the frame-sync error memory.

5. An error flag generation method comprising:

receiving a reproduced digital signal;

generating frame-sync error information for at least one data block using the reproduced digital signal;

storing the frame-sync error information in a frame-sync error memory for the at least one data block;

generating a BIS error flag for the at least one data block;

storing the BIS error flag in a BIS error flag memory for the at least one data block; and

generating an error flag indicating error existence/absence for ECC data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

6. The method of claim 5, wherein the frame-sync error memory stores frame-sync error information corresponding to at least two data blocks.

7. The method of claim 5, wherein the at least one data block has an error correction format in which frame-sync data is recorded in a heading of the at least one data block and BIS data columns are recorded respectively between sets of ECC data columns, and the generating of the error flag comprises generating an error flag indicating the error existence for entire ECC data constructing a set of ECC data columns, with reference to error information stored in the frame-sync error memory and the BIS error flag memory, if both the frame-sync error information of the frame-sync data and the BIS error flag of a BIS data column neighboring the set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring the set of the ECC data columns, indicate error existence.

8. An apparatus generating an error flag, comprising:

a frame-sync detector, outputting frame-sync error information indicating an existence/absence of an error for frame sync-data of frames forming data blocks;

a frame-sync error memory, storing the frame-sync error information of the frames forming the data blocks;

a BIS (Burst Indicator Subcode) error flag memory, storing a BIS error flag for the data blocks; and

an error flag generator, generating an error flag indicating an existence/absence of an error for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

9. The apparatus of claim 8, wherein the frame-sync error memory stores frame-sync error information corresponding to at least two data blocks.

10. The apparatus of claim 8, wherein the BIS error flag memory stores BIS error flag corresponding to at least two data blocks.

11. The apparatus of claim 8, wherein the frame-sync error memory comprises a first through N-th frame-sync error memories.

12. The apparatus of claim 11, wherein N is at least two.

13. The apparatus of claim 11, wherein each of the frame-sync error memories has a size of 1x496 bits, and stores frame-sync error information of at least one data block.

14. The apparatus of claim 8, wherein the BIS error flag memory comprises a first through an M-th BIS error memories.

15. The apparatus of claim 14, wherein M is at least two.

16. The apparatus of claim 14, each of the BIS error memories has a size of 1x496 bits, and stores BIS error flag of at least one data block.

17. The apparatus of claim 8, wherein each of the data blocks has an error correction format in which frame-sync data is recorded in a heading of the data block and BIS data columns are recorded between sets of ECC data columns.

18. The apparatus of claim 17, wherein the error flag generator, generates an error flag indicating the existence of an error for an entire ECC data forming a set of ECC data columns with reference to error information stored in the frame-sync error memory and the BIS error flag memory, if the frame-sync error information of the frame-sync data and the BIS error flag of the BIS data column neighboring a set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring a set of the ECC data columns, indicate error existence.